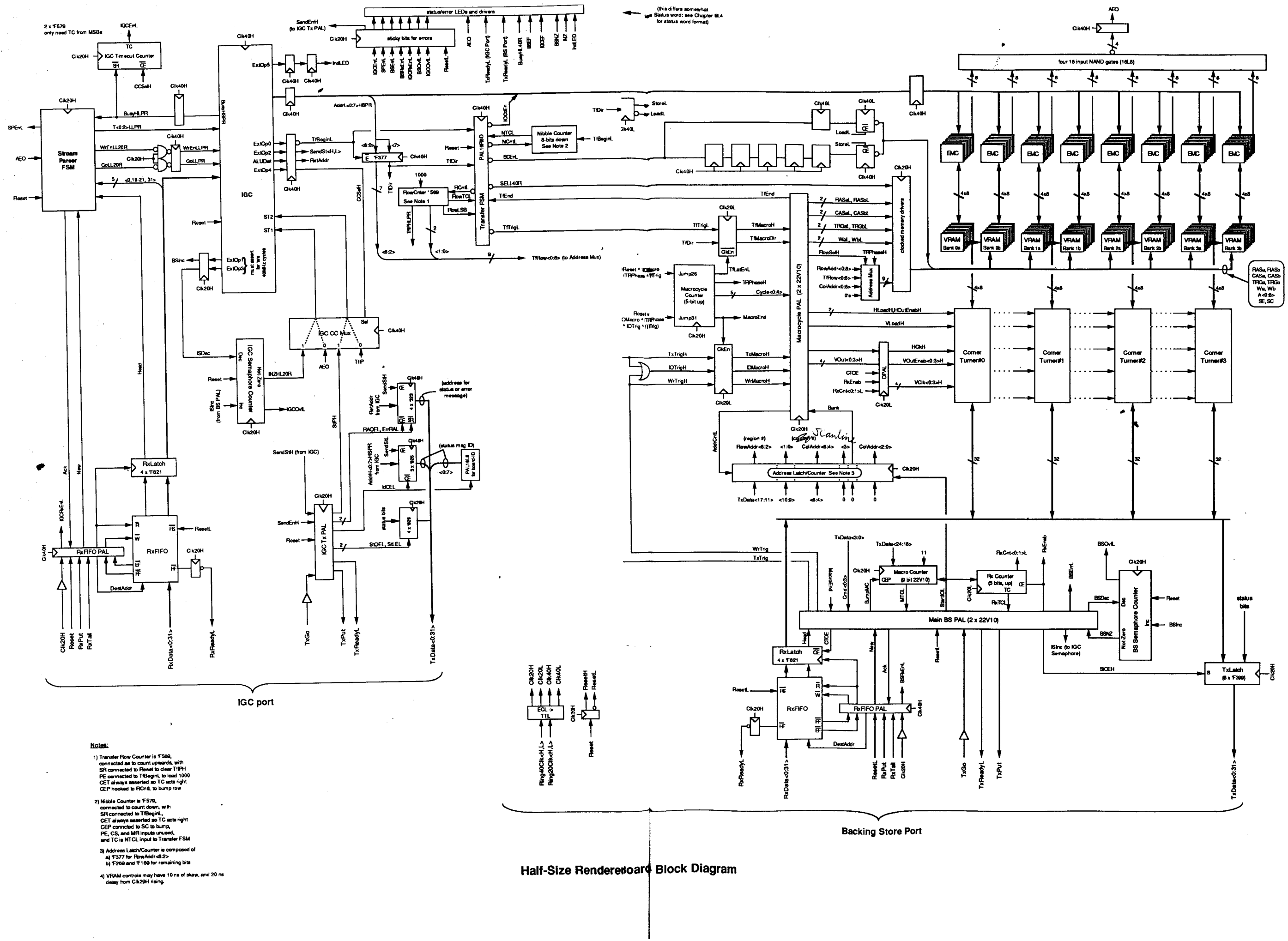

Notes:

1) Transfer Row Counter is F569,
connected as to count upwards, with
SR connected to Reset to clear TfIPH
PE connected to TfBeginL to load 1000
CET always asserted as TC acts right
CEP hooked to RCntL to bump row

2) Nibble Counter is F579,
connected to count down, with
SR connected to TfBeginL,
CET always asserted as TC acts right
CEP connected to SC to bump,
PE, CS, and MR inputs unused,
and TC is NTCL input to Transfer FSM

3) Address Latch/Counter is composed of
a) F377 for RowAddr<8:2>
b) F269 and F169 for remaining bits

4) VRAM controls may have 10 ns of skew, and 20 ns
delay from Clk20H rising.

Half-Size Renderer Board Block Diagram