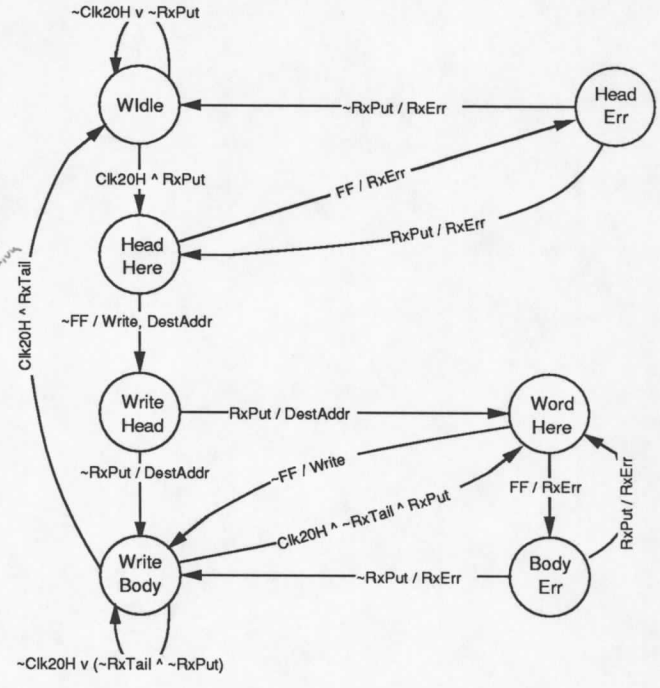
State Diagram for Rx FIFO Write PAL

(identical for BS and IGC ports)

PAL is clocked by Clk40H (rising edge).
Asserts "DestAddr" marker on spare FIFO bit with destination address (assuming destination address is valid on the cycle after first RxPut following Reset or RxTail.
If FIFO is full and ring asserts RxPut, an RxErr error is generated, and the word is skipped. If skipped word was destination address, DestAddr is asserted with first data word which is successfully written.
If no errors occur, one word is written into FIFO for every RxPut.
Nothing is written into FIFO for RxTail.
Note than ring signals RxPut and RxTail are mutually exclusive, and are sampled only near the end of the high half of the Clk20H cycle.
FIFO full flag (FF) is valid a setup time prior to the rising edge of Clk40H which occurs at the end of the low half of Clk20H cycle.

so needn't worry about missing PAL hold-time if tpd=minimum

Note: 'Reset' input causes immediate jump to Idle state (WIdle or RIdle) with all outputs de-asserted. All other transitions implicitly assume ~Reset.



Inputs:

- Reset - unconditonally resets to Idle state
- Clk20H - 20 MHz TTL clock
- RxPut - indicates packet destination address or data word valid on next Clk20H cycle
- FF - (active low) indicates FIFO is full; writing to a full FIFO generates RxErr
- RxTail - asserted after last word of message, before first RxPut of next message

Outputs:

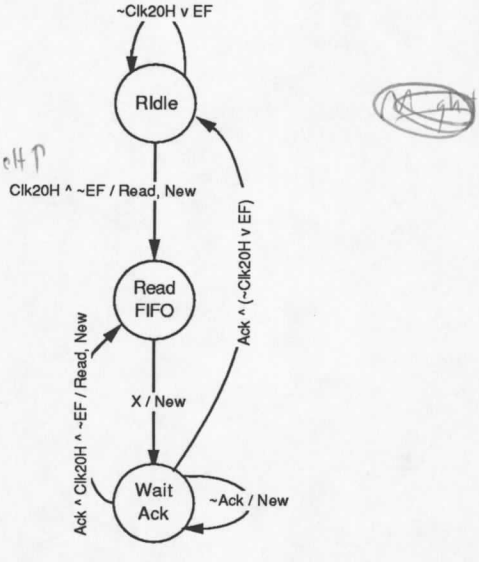
- Write - assert active low write pulse for FIFO, is may only be asserted during high phase of Clk20H
- DestAddr - asserted into spare FIFO input with destination address of packet
- RxErr - assert active low RxErrL error strobe, occurs whenever full FIFO prevents a Write, asserted for one Clk20H cycle

State Diagram for Rx FIFO Read PAL

(identical for BS and IGC ports)

PAL is clocked by Clk40H (rising edge).
FIFO empty flag (EF) is valid a setup time prior to the rising edge of Clk40H which occurs at the end of the high half of Clk20H cycle.
When a word is read, New is asserted. New remains asserted, and data stays valid on RxLatch, until recepient asserts Ack. Recepient need only assert Ack for one 20 MHz cycle, and New will be re-asserted when next word is ready (or remain asserted if next word is ready immediately). The old word remains valid during the 20 MHz cycle during which Ack is first asserted.

Ack must be valid 10ns before all Clk40H edges!

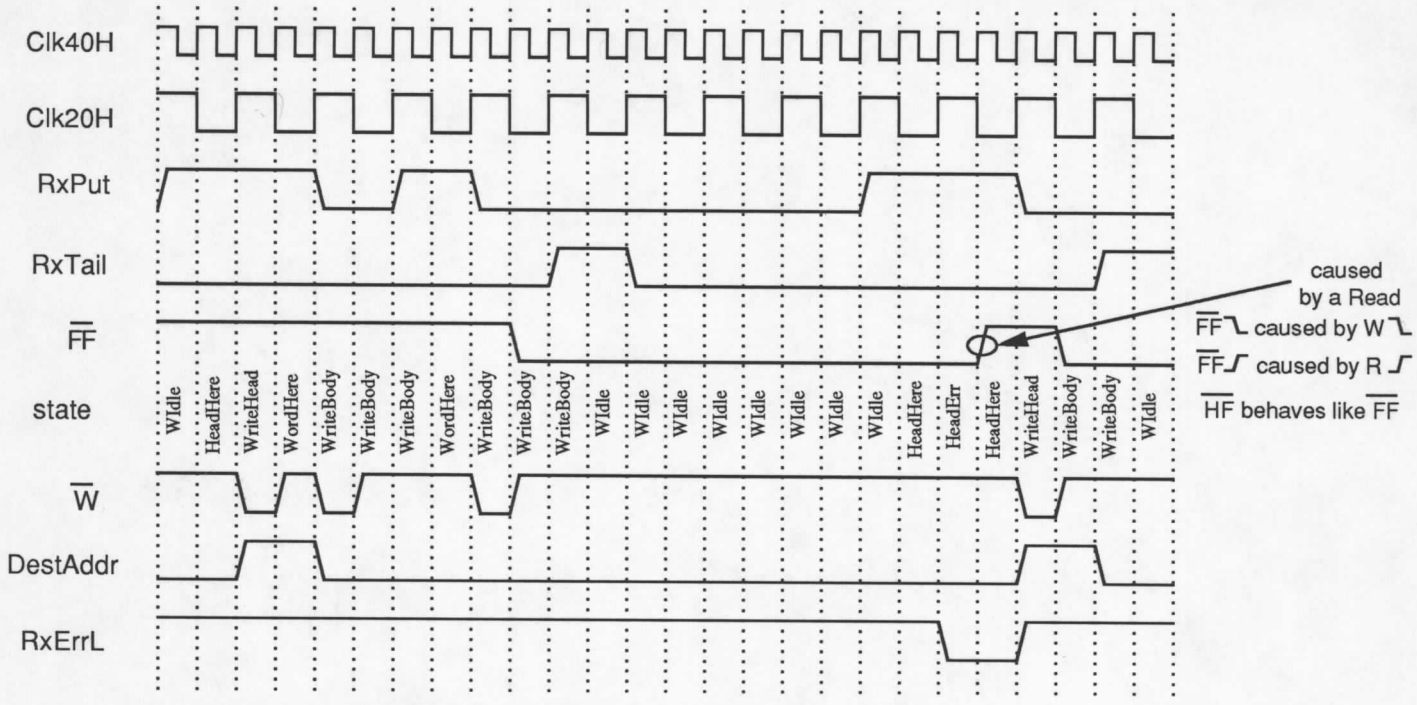


Inputs:

- Reset - unconditonally resets to Idle state
- Clk20H - 20 MHz TTL clock, aligned with Clk40H
- EF - (active low) indicates FIFO is empty
- Ack - recepient asserts if ready for another word on the next Clk20H cycle, should be latched on rising edge of Clk20H

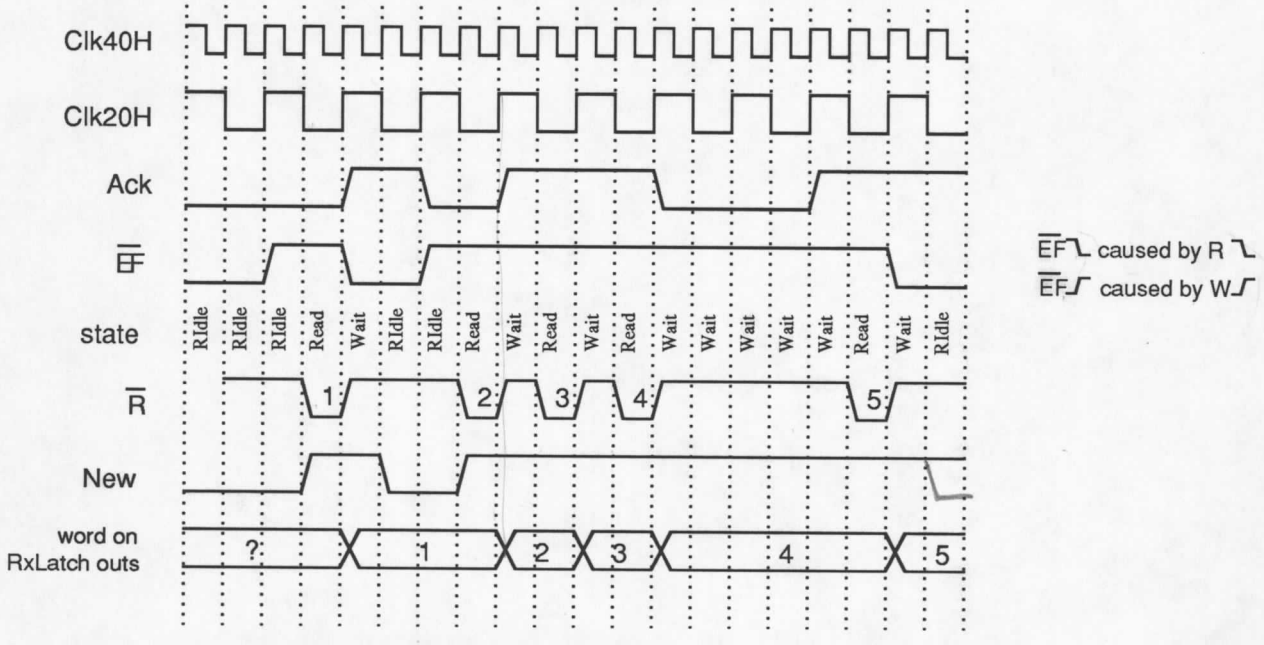
Outputs:

- Read - active low Read pulse for FIFO, is asserted only during low phase of Clk20H
- New - asserted with Read to notify recepient that next word will be ready starting with next Clk20H cycle



FIFO Write Timing Example

Shows a 2 word (plus dest-addr) message being received and written into FIFO, followed by a 1 word message in which the dest-addr is missed (generating an error) so the Head bit is attached to the data word.



FIFO Read Timing Example

Word #1 is Read, wait a cycle for empty FIFO, Read words 2, 3, and 4, wait two cycles for Ack of word #4, Read word #5, FIFO is empty again.

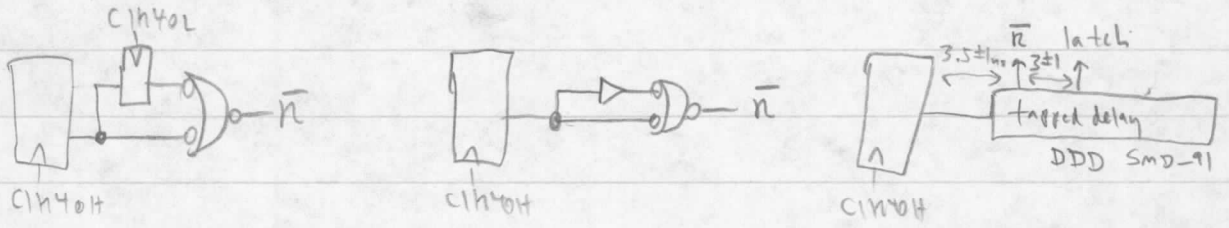
Note that Read PAL has no concept of beginning and ending of messages; it just passes the Head bit as a 33rd data bit.

Other Approaches for FIFO Read/Write 13-Sep-89

(1) use AMD 674219, converts SRAM into FIFO
TOO SLOW!

(2) use separate counter to generate my own FF, EF, HF flags; so can use ~35ns w/ delay line + not have to worry about flag I being too late

(3) interleave 2 FIFO's, still must retain current ch → Read → ValidData timing



Problems: must generate 25 ns read pulse, $\overline{R}\downarrow$ must be early enough to guarantee $\overline{EF}\downarrow$ soon enough for next read decision; $\overline{R}\uparrow$ must be early enough that data ready for C.T. input in time; and latch signal (for RxLatch) must allow setup/hold of valid data

remember: must be able to read BJ FIFO at 20MHz, and must be able to write both at 20MHz; no point in pulling trick w/ IDT FIFO (i.e. 1 read every 3 40MHz cycles), since the BJ is really the one that needs to be deeper than 1K